Claim Listing

Please cancel claims 14-21.

1. (Currently Amended) A ~~microprocessor control apparatus for uniformly reducing processor power independent of the processor logic~~ processing system, comprising:

~~a full power state machine control input;~~

~~a nap state machine control input;~~

~~a state machine ramp control;~~

~~a delay counter;~~

~~a pulse train generator;~~

~~a multiplexer;~~

~~a timed clock distribution control network;~~

~~a local clock buffer;~~

~~a full power state machine control input controlling the 'ramp down' request;~~

~~a nap state machine control input controlling the 'not ramp down' request input;~~

~~a full power state machine control input and a nap state machine control input coupled to a state machine ramp control;~~

~~a state machine ramp control connected to a delay counter and coupled to a pulse train generator;~~

~~a pulse train generator supplying and mixing pulses through a multiplexer connected to a timed clock control distribution network; and~~

~~a timed clock control distribution network coupled to a local clock buffer~~

a processor comprising logic coupled to receive a clock signal via a plurality of local clock buffers, wherein the processor is configured to operate in a first power mode and a second power mode, and wherein the processor dissipates different amounts of electrical power in the first and second power modes;

a pulse train generator configured to produce three or more pulse trains, wherein each of the three or more pulse trains corresponds to a different level of electrical power dissipation within the processor;

selection logic coupled to receive each of the pulse trains produced by the pulse train generator and configured to produce a selected one of the pulse trains;

control logic coupled to the selection logic and configured to control the selection logic to effect transitions between the first and second power modes, wherein during each transition between the first and second power modes the selection logic produces at least three of the three or more pulse trains produced by the pulse train generator in sequence such that the electrical power dissipation of the processor changes monotonically during the transition; and

a timed clock control distribution network coupled to receive the sequence of pulse trains produced by the selection logic and configured to provide the sequence of pulse trains to the local clock buffers such that each of the local clock buffers receives the sequence of pulse trains at the same time.

2. (Currently Amended) The processing system of claim 1, wherein ~~the nap interrupt device is coupled to the state machine ramp control through the ramp down request module~~ the processor dissipates more electrical power in the first power mode than in the second power mode.

3. (Currently Amended) The processing system of claim ~~1~~ 2, wherein ~~a pulse train generator further comprises a delay counter unit and a state machine ramp control unit, wherein the pulse train generator is employed to transmit the pulse train to the timed clock control signal distribution network~~ the pulse train generator is configured to produce a constant high pulse train having a constant high voltage level, a constant low pulse train having a constant low voltage level, and one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level.

4. (Currently Amended) The processing system of claim ~~1~~ 3, ~~further comprising a local clock buffer control device employed to exercise control of the processor by means of conditioning the clock signal~~ wherein when the processor is operating in the first power mode, the selection logic produces the constant low pulse train, and wherein when the processor is operating in the second power mode the selection logic produces the constant high pulse train.

5. (Currently Amended) The processing system of claim ~~1~~ 4, wherein ~~the pulse trains from the pulse train generator drive the local clock buffer devices~~ during a transition from the first power mode to the second power mode, the selection logic produces the constant low pulse train, at least one of the one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level, and the constant high pulse train in sequence such that the electrical power dissipation of the processor decreases monotonically during the transition.

6. (Currently Amended) The processing system of claim ~~1~~ 5, ~~further comprising an external power analysis, wherein processor clocking power is analyzed for power requirements for all processor processes~~ wherein during a transition from the second power mode to the first power mode, the selection logic produces the constant high pulse train, at least one of the one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level, and the constant low pulse train in sequence such that the electrical power dissipation of the processor increases monotonically during the transition.

7. (Currently Amended) The processing system of claim ~~3~~ 1, wherein ~~the ramp down request device includes a signal device between the processor and the state machine ramp control to transmit the 'go to nap' command~~ during a transition from the second power mode to the first power mode, the selection logic produces at least three of the three or more pulse trains produced by the pulse train generator in sequence such that the electrical power dissipation of the processor increases monotonically during the transition.

8. (Currently Amended) The processing system of claim ~~3~~ 1, wherein ~~the counter to create delay for next step unit includes an input/output loop to transmit signals to the state machine control ramp during a time period when the ramp down request is active~~ each of the local clock buffers is coupled to receive the clock signal and the sequence of pulse trains from the timed clock control distribution network, and configured to provide the clock signal to the logic of the processor dependent upon the sequence of pulse trains.

9. (Currently Amended) The processing system of claim [[4]] 1, wherein ~~a local clock buffer device conditions a latch at a processor node~~ the control logic comprises a state machine ramp control system and a delay counter coupled to the state machine ramp control system.

10. (Currently Amended) The processing system of claim [[3]] 9, wherein ~~one or more devices can include a programmable memory storage device or input device~~ the state machine ramp is configured to cycle and reset the delay counter, and wherein the delay counter comprises a plurality of programmable storage elements and a plurality of comparison elements, and wherein each of the storage elements is configured to store a delay value, and wherein each of the comparison elements is coupled to a corresponding one of the storage elements, and wherein each of the comparison elements is coupled to receive a counter value and a delay value from the corresponding storage element, and is configured to produce a signal in the event the counter value matches the delay value.

11. (Currently Amended) ~~A method for performing a plurality of shifts in clock frequency~~ In a processing system comprising a processor coupled to receive a clock signal and configured to operate in a first power mode and a second power mode, a method for transitioning between the first and second power modes, the method comprising:

~~initiating a ramp down request as a function of a change in a power interrupt request;~~

~~incrementing a counter to start a state machine ramp control;~~

~~initiating a state machine ramp control logic;~~

~~selecting a pulse train from a pulse train generator;~~

~~masking a clocking power signal;~~

~~fanning out a pulse train;~~

~~driving a pulse train to the local clock buffers;~~

~~substantially halting a processor with a constant low signal; and~~

~~substantially restarting a processor at full power with a constant high signal~~

producing three or more pulse trains each corresponding to a different level of electrical power dissipation within the processor;

during a transition between the first and second power modes, producing at least three of the three or more pulse trains in sequence such that the electrical power dissipation of the processor changes monotonically during the transition; and

providing the sequence of pulse trains to each of a plurality of local clock buffers such that each of the local clock buffers receives the sequence of pulse trains at the same time, wherein each of the local clock buffers is coupled to receive the clock signal and the sequence of pulse trains, and configured to provide the clock signal to the processor dependent upon the sequence of pulse trains.

12. (Currently Amended) The method of claim 11, wherein ~~a pulse train is selected by a specific state within a state machine control ramp~~ the producing the three or more pulse trains comprises:

producing three or more pulse trains comprising: a constant high pulse train having a constant high voltage level, a constant low pulse train having a constant low voltage level, and one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level.

13. (Currently Amended) The method of claim ~~11~~ 12, wherein ~~a selected pulse train is multiplexing and masking a clocking power signal~~ the producing the at least three of the three or more pulse trains in sequence comprises:

during a transition between the first and second power modes, producing a first constant level pulse train, at least one of the one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level, and a second constant level pulse train in sequence such that the electrical power dissipation of the processor changes monotonically during the transition.

14-21 (Canceled.)

Please add the following new claims:

22. (Newly Added) A processing system, comprising:

a processor comprising logic coupled to receive a clock signal via a plurality of local clock buffers, wherein the processor is configured to operate in a first power mode and a second power mode, and wherein the processor dissipates different amounts of electrical power in the first and second power modes;

a pulse train generator configured to produce three or more pulse trains comprising: a first constant pulse train having a constant first voltage level, a second constant pulse train having a constant second voltage level, and one or more pulse trains that alternate between the first and second voltage levels, wherein each of the three or more pulse trains corresponds to a different level of electrical power dissipation within the processor;

selection logic coupled to receive each of the pulse trains produced by the pulse train generator and configured to produce a selected one of the pulse trains;

control logic coupled to the selection logic and configured to control the selection logic to effect transitions between the first and second power modes, wherein during each transition between the first and second power modes the selection logic produces at least three of the three or more pulse trains produced by the pulse train generator in sequence such that the electrical power dissipation of the processor changes monotonically during the transition; and

a timed clock control distribution network coupled to receive the sequence of pulse trains produced by the selection logic and configured to provide the sequence of pulse trains to the local clock buffers such that each of the local clock buffers receives the sequence of pulse trains at the same time.

23. (Newly Added) The processing system of claim 22, wherein the processor dissipates more electrical power in the first power mode than in the second power mode.

24. (Newly Added) The processing system of claim 23, wherein when the processor is operating in the first power mode, the selection logic produces the second constant pulse train, and wherein when the processor is operating in the second power mode the selection logic produces the first constant pulse train.

25. (Newly Added) The processing system of claim 24, wherein during a transition from the first power mode to the second power mode, the selection logic produces the second constant pulse train,

at least one of the one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level, and the first constant pulse train in sequence such that the electrical power dissipation of the processor decreases monotonically during the transition.

26. (Newly Added) The processing system of claim 25, wherein during a transition from the second power mode to the first power mode, the selection logic produces the first constant pulse train, at least one of the one or more pulse trains that alternate between the constant high voltage level and the constant low voltage level, and the second constant pulse train in sequence such that the electrical power dissipation of the processor increases monotonically during the transition.

27. (Newly Added) The processing system of claim 26, wherein the first voltage level is greater than the second voltage level.

28. (Newly Added) The processing system of claim 1, wherein each of the local clock buffers is coupled to receive the clock signal and the sequence of pulse trains from the timed clock control distribution network, and configured to provide the clock signal to the logic of the processor dependent upon the sequence of pulse trains.